

WATCHDOG SYSTEM AND METHOD FOR  
MONITORING FUNCTIONALITY OF A PROCESSOR

ABSTRACT OF THE DISCLOSURE

[0042] The present invention provides watchdog system and method for monitoring the functionality of a processor in communication with the watchdog. In at least one embodiment of the invention, a system of monitoring the functionality of a processor is provided employs a boot up timer, a forbidden timer, an acknowledgement timer, and a cycle period timer. A certain number of acknowledgement signals are expected from the processor at predetermined times in order for the processor to escape reset. For example, a reset signal is asserted to the processor if any one of the following conditions are met: (i) not receiving an acknowledgement signal prior to the expiration of the boot up timer; (ii) receiving an acknowledgement signal prior to the expiration of the acknowledgement timer; (iii) receiving an acknowledgement signal prior to the expiration of the forbidden timer, and (iv) not receiving all of the acknowledgement signals prior to the expiration of the cycle period timer.